19-3466; Rev 2; 2/08

EVALUATION KIT AVAILABLE

TMDS Digital Video Equalizer for DVI/HDMI Cables

MAX3815

General Description

The MAX3815 cable equalizer automatically provides compensation for DVI™, HDMI™, DFP, PanelLink®, and ADC cables. It extends the usable cable distance up to 36 meters. The MAX3815 is designed to equalize signals encoded in the transition-minimized differential signaling (TMDS®) format.

The MAX3815 features four CML-differential inputs and outputs (three data and one clock). It provides a loss-of-signal (LOS) output that indicates loss-of-clock signal. The outputs include a disable function or the equalizer can be powered down to conserve power. For direct chip-to-chip communication, the output drivers can be switched to one-half the DVI output specification to conserve power and reduce EMI. Equalization can be automatic or set to manual control for specific in-cable applications.

The MAX3815 is available in a 7mm x 7mm, 48-pin TQFP-EP package and operates over a 0°C to +70°C temperature range.

Applications

Front-Projector DVI/HDMI Inputs

High-Definition Televisions and Displays

DVI-D/HDMI Cable-Extender Modules and Active Cable Assemblies

LCD Computer Monitors

Pin Configuration appears at end of data sheet.

Features

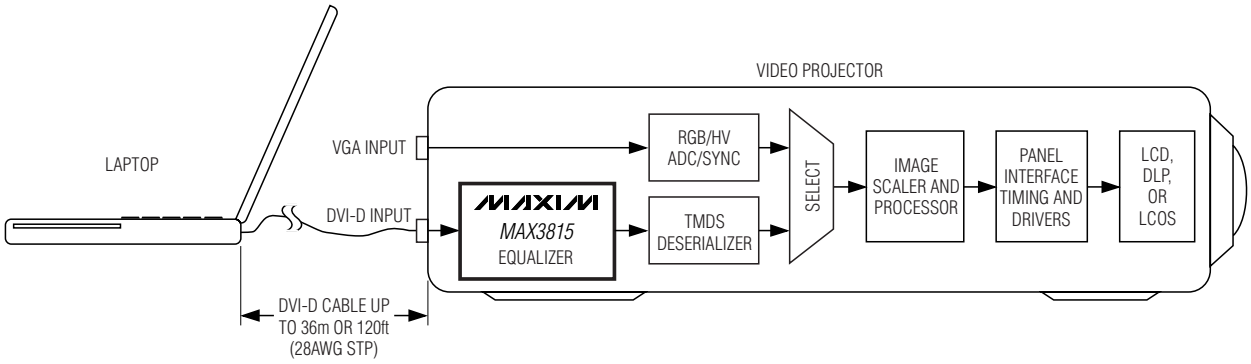
- **Extends TMDS Cable Reach to Projectors or Monitors Using DVI, DFP, PanelLink, ADC, or HDMI Interfaces**
- **Extends TMDS Interface Length as Follows:**
  0 to 50 Meters Over DVI-Cable, 24 AWG STP (Shielded-Twisted Pair)
  0 to 36 Meters Over DVI-Cable, 28 AWG STP
  0 to 30 Meters Over DVI-Cable, 30 AWG STP
- **Compatible with DTV Resolutions 480i, 480p, 720p, 1080i, and 1080p**
- **Compatible with Computer Resolutions VGA, SVGA, XGA, SXGA, UXGA**
- **Fully Automatic Equalization Up to 40dB at 825MHz (1.65Gbps), No System Control Required**
- **3.3V Power Supply**
- **Power Dissipation of 0.6W (typ)**
- **7mm x 7mm 48-Pin TQFP Lead-Free Package**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX3815CCM	0°C to +70°C	48 TQFP-EP*	C48E-8
MAX3815CCM+	0°C to +70°C	48 TQFP-EP*	C48E-8

+Denotes lead-free package.
**EP = Exposed pad.*

Typical Application Circuits



Typical Application Circuits continued at end of data sheet.

DVI is a trademark of Digital Display Working Group.
HDMI is a trademark of HDMI Licensing, LLC.
PanelLink and TMDS are registered trademarks of Silicon Image, Inc.

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

TMDS Digital Video Equalizer for DVI/HDMI Cables

ABSOLUTE MAXIMUM RATINGS

Supply Voltage V_{CC} .....-0.5V to +4.0V
Voltage at All I/O Pins.....-0.5V to (V_{CC} + 0.7V)
Voltage between any CML I/O Complementary Pair .....±3.3V
Continuous Power Dissipation (T_A = +70°C)
48-Pin TQFP-EP (derate 36.2mW/°C above +70°C) ..2896mW
Operating Junction Temperature Range.....-55°C to +150°C
Storage Temperature Range .....-55°C to +150°C
Die Attach Temperature.....+400°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +3.6V, T_A = 0°C to +70°C. Typical Values are at V_{CC} = +3.3V, external terminations = 50Ω ±1%, TMDS rate = 250Mbps to 1.65Gbps, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Power-Supply Current	I_{CC}	$\overline{PWRDWN}$ = HIGH			165	230	mA
		$\overline{PWRDWN}$ = LOW			10		
Supply-Noise Tolerance		DC to 500kHz			200		mV_{P-P}
EQUALIZER PERFORMANCE							
Residual Output Jitter (Cables Only) 0.25Gbps to 1.65Gbps (Notes 1, 2, and 3)		1dB skin-effect loss at 825MHz				0.2	UI
		24dB skin-effect loss at 825MHz				0.2	
		40dB skin-effect loss at 825MHz				0.2	
CID Tolerance				20			Bits
CONTROL AND STATUS							
$\overline{CLKLOS}$ Assert Level		Differential peak-to-peak at EQ input with 165MHz clock			50		mV_{P-P}
CML INPUTS (CABLE SIDE)							
Differential Input Voltage Swing	V_{ID}	At cable input		800	1000	1400	mV_{P-P}
Common-Mode Input Voltage	V_{CM}			V_{CC} - 0.4		V_{CC} + 0.1	V
Input Resistance	R_{IN}	Single-ended		45	50	55	Ω
CML OUTPUTS (ASIC SIDE)							
Differential Output-Voltage Swing	V_{OD}	50Ω load, each side to V_{CC}	OUTLEVEL = HIGH	800	1000	1200	mV_{P-P}
			OUTLEVEL = LOW	350	500	650	
Output-Voltage High		Single-ended, OUTLEVEL = HIGH			V_{CC}		mV
Output-Voltage Low		Single-ended, OUTLEVEL = HIGH		V_{CC} - 600		V_{CC} - 400	mV
Output Voltage During Power-Down		Single-ended, $\overline{PWRDWN}$ = LOW		V_{CC} - 10		V_{CC} +10	mV

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +3.0V to +3.6V, T_A = 0°C to +70°C. Typical Values are at V_{CC} = +3.3V, external terminations = 50Ω ±1%, TMDS rate = 250Mbps to 1.65Gbps, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Common-Mode Output Voltage		50Ω load, each side to V_{CC}, OUTLEVEL = HIGH		V_{CC} - 0.25		V
Rise/Fall Time (Note 1)		20% to 80%	80	130	200	ps
LVTTL CONTROL AND STATUS INTERFACE						
LVTTL Input High Voltage	V_{IH}		2.0			V
LVTTL Input Low Voltage	V_{IL}				0.8	V
LVTTL Input High Current		$V_{IH(MIN)} < V_{IN} < V_{CC}$			-50	µA
LVTTL Input Low Current		GND < V_{IN} < $V_{IL(MAX)}$			-100	µA
Open-Collector Output High		R_{LOAD} ≥ 10kΩ to V_{CC}	2.4			V
Open-Collector Output Low		R_{LOAD} ≥ 2kΩ to V_{CC}			0.4	V
Open-Collector Output Sink					5	mA

Note 1: AC specifications are guaranteed by design and characterization.

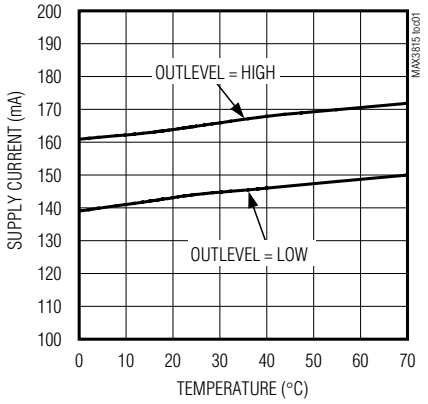
Note 2: Cable input swing is 800mV to 1400mV differential peak-to-peak. Residual output jitter is defined as peak-to-peak deterministic jitter + 14.2 times random jitter.

Note 3: Test pattern is a 2^7 - 1 PRBS + 20 ones + 2^7 - 1 PRBS (inverted) + 20 zeros.

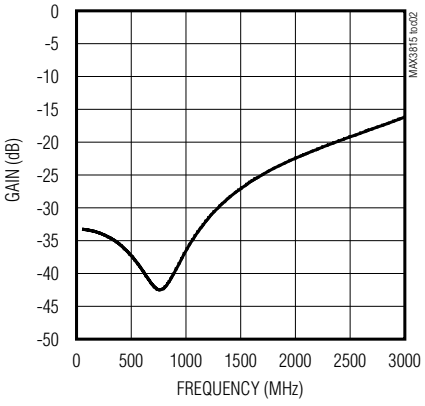
Typical Operating Characteristics

(Typical values are at V_{CC} = +3.3V, T_A = +25°C, data pattern = 2^7 - 1 PRBS + 20 ones + 2^7 - 1 PRBS (inverted) + 20 zeros, unless otherwise noted.)

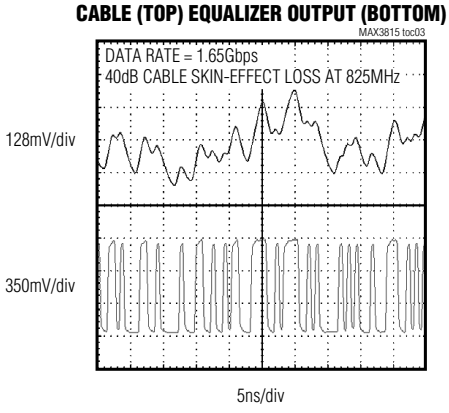
SUPPLY CURRENT vs. TEMPERATURE



DIFFERENTIAL INPUT RETURN LOSS vs. FREQUENCY



EQUALIZER INPUT AFTER 205ft OF GORE 89 CABLE (TOP) EQUALIZER OUTPUT (BOTTOM)

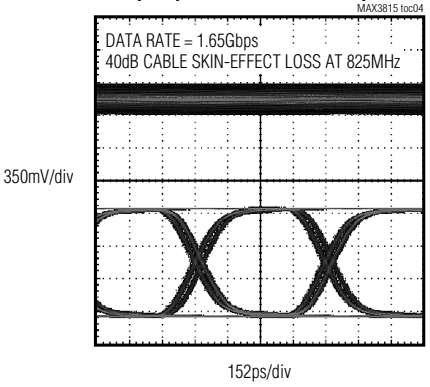


TMDS Digital Video Equalizer for DVI/HDMI Cables

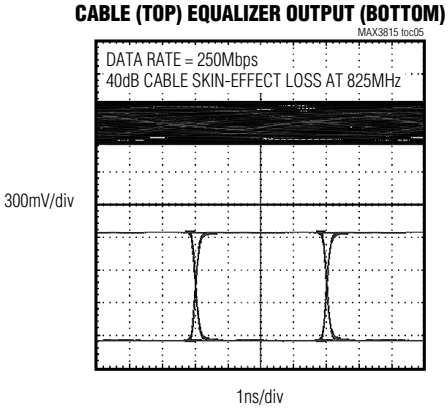
Typical Operating Characteristics (continued)

(Typical values are at V_{CC} = +3.3V, T_A = +25°C, data pattern = 2^7 - 1 PRBS + 20 ones + 2^7 - 1 PRBS (inverted) + 20 zeros, unless otherwise noted.)

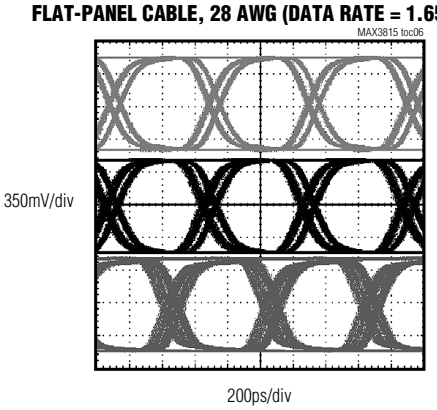
EQUALIZER INPUT EYE AFTER 205ft OF GORE 89 CABLE (TOP) EQUALIZER OUTPUT (BOTTOM)



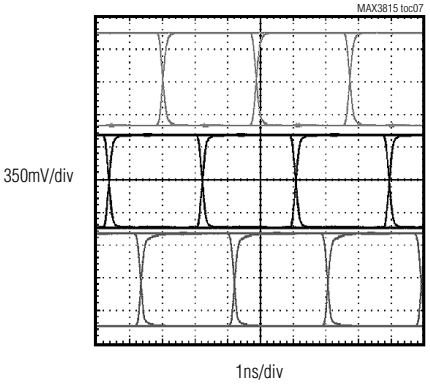
EQUALIZER INPUT EYE AFTER 205ft OF GORE 89 CABLE (TOP) EQUALIZER OUTPUT (BOTTOM)



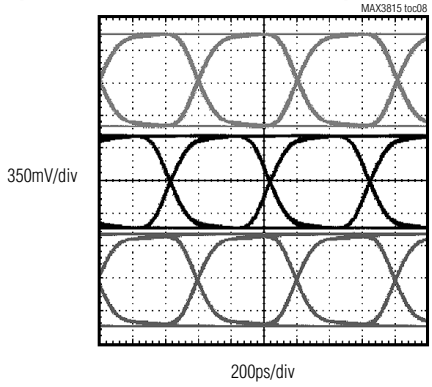
EQUALIZER EYES AFTER 100ft MADISON DIGITAL FLAT-PANEL CABLE, 28 AWG (DATA RATE = 1.65Gbps)



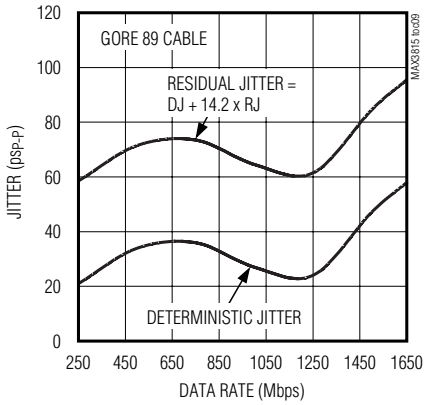
EQUALIZER EYES AFTER 100ft MADISON DIGITAL FLAT-PANEL CABLE, 28 AWG (DATA RATE = 350Mbps)



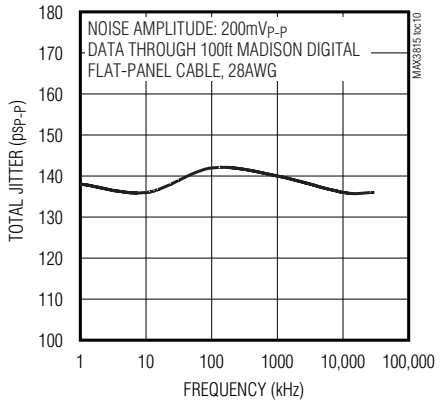
EQUALIZER EYES AFTER 3ft CABLE (DATA RATE = 1.65Gbps)



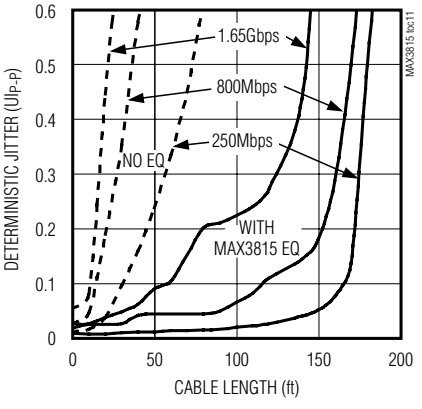
JITTER vs. DATA RATE AFTER 205ft CABLE WITH 40dB SKIN-EFFECT LOSS AT 825MHz



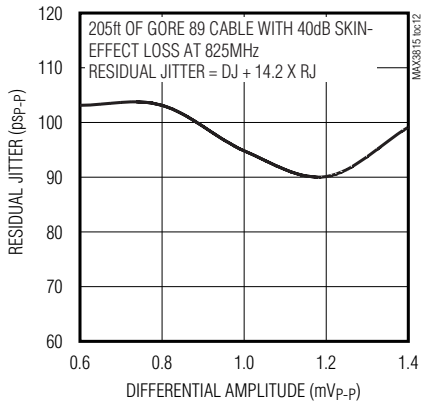
TOTAL JITTER vs. POWER-SUPPLY NOISE FREQUENCY (DATA RATE = 1.65Gbps)



DETERMINISTIC JITTER vs. CABLE LENGTH (TENSOLITE TWIN-AX 28 AWG)



RESIDUAL JITTER vs. SIGNAL AMPLITUDE INPUT TO CABLE (DATA RATE = 1.65Gbps)

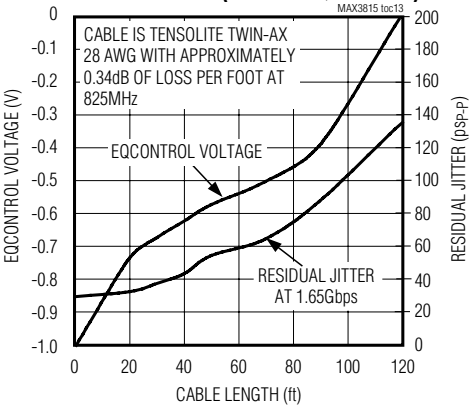


TMDS Digital Video Equalizer for DVI/HDMI Cables

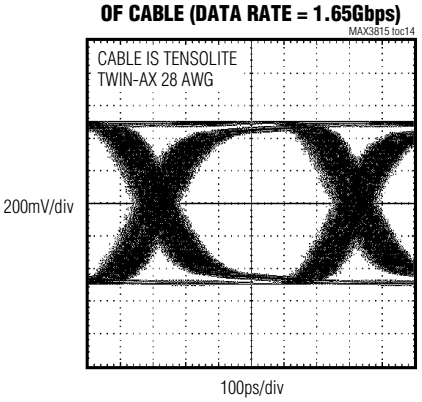
Typical Operating Characteristics (continued)

(Typical values are at V_{CC} = +3.3V, T_A = +25°C, data pattern = 2^7 - 1 PRBS + 20 ones + 2^7 - 1 PRBS (inverted) + 20 zeros, unless otherwise noted.)

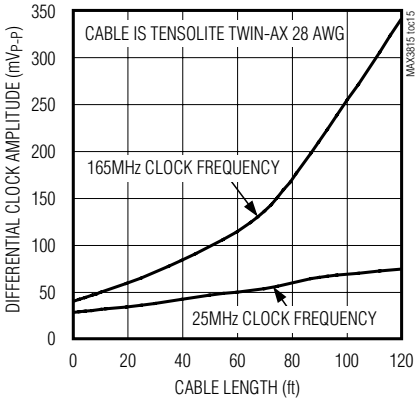
EQCONTROL VOLTAGE (RELATIVE TO V_{CC}) vs. CABLE LENGTH (MANUAL EQ CONTROL)



EQUALIZER OUTPUT EYE AFTER 120ft OF CABLE (DATA RATE = 1.65Gbps)



LOSS-OF-CLOCK ASSERT THRESHOLD vs. CABLE LENGTH



Pin Description

PIN	NAME	FUNCTION
1, 4, 5, 8, 9, 12, 13, 16, 38, 41, 43, 44	V_{CC}	Supply Voltage. All pins must be connected to V_{CC}.
2	RX0_IN-	Negative Data Input, CML
3	RX0_IN+	Positive Data Input, CML
6	RX1_IN-	Negative Data Input, CML
7	RX1_IN+	Positive Data Input, CML
10	RX2_IN-	Negative Data Input, CML
11	RX2_IN+	Positive Data Input, CML
14	RXC_IN+	Positive Clock Input, CML
15	RXC_IN-	Negative Clock Input, CML
17	EQCONTROL	Equalizer Control. This pin allows the user to control the equalization level of the MAX3815. Connect the pin to GND for automatic operation. Set the voltage to V_{CC} / 2 for minimum equalization, or set the voltage between V_{CC} - 1V to V_{CC} for manual equalization. See the *Typical Operating Characteristics* for more information.
18	$\overline{CLKLOS}$	Loss-of-Clock Signal Output, LVTTL Open Collector. This pin asserts low upon loss of the input TMDS clock from the cable.
19	$\overline{PWRDWN}$	Power-Down Input, LVTTL. This input allows the IC to be powered down to conserve power. Connect high for normal operation. Pull low for power-down mode.

TMDS Digital Video Equalizer for DVI/HDMI Cables

Pin Description (continued)

PIN	NAME	FUNCTION
20, 23, 24, 25, 28, 29, 32, 33, 36, 37, 42	GND	Ground
21	RXC_OUT-	Negative Clock Output, CML
22	RXC_OUT+	Positive Clock Output, CML
26	RX2_OUT+	Positive Data Output, CML
27	RX2_OUT-	Negative Data Output, CML
30	RX1_OUT+	Positive Data Output, CML
31	RX1_OUT-	Negative Data Output, CML
34	RX0_OUT+	Positive Data Output, CML
35	RX0_OUT-	Negative Data Output, CML
39	OUTLEVEL	Output-Level Control Input, LVTTL. This input sets the output amplitude to the standard DVI level (1000mV$_{P-P}$) when high, and sets the output amplitude to 1/2 the DVI level (500mV$_{P-P}$) when low.
40	$\overline{OUTON}$	Output-Enable Control Input, LVTTL. This input enables the CML outputs when forced low and sets a differential logic zero when forced high.
45–48	N.C.	No Connection
EP	Exposed Pad	Ground. The exposed pad must be soldered to the circuit-board ground for proper thermal and electrical operation.

Detailed Description

The MAX3815 TMDS equalizer accepts differential CML input data at rates of 250Mbps up to 1.65Gbps (individual channel data rate). It automatically adjusts to attenuation levels of up to 40dB at 825MHz due to skin-effect losses in copper cable. It consists of four CML input buffers, a loss-of-clock signal detector, three independent adaptive equalizers, four limiting amplifiers, and four output buffers (Figure 1).

CML Input Buffers and Output Drivers

The input buffers and the output drivers are implemented using current-mode logic (CML) (see Figures 3 and 4). The output drivers are open-collector and can be turned off with the $\overline{OUTON}$ pin, or can be set to output a one-half amplitude signal (500mV$_{P-P}$ differential) using the OUTLEVEL pin. For details on interfacing with CML, refer to Maxim Application Note *HFAN-01.0: Introduction to LVDS, PECL, and CML*.

Loss-of-Clock Signal Detector

The loss-of-clock signal detector indicates a loss-of-clock signal at the $\overline{CLKLOS}$ pin.

Adaptive Equalizer

The three data channels each contain an independent adaptive equalizer. Each channel analyzes the incoming signal and determines the amount of equalization to apply.

Limiting Amplifier

The limiting amplifier amplifies the signal from the adaptive equalizer and truncates the top and bottom of the waveform to provide a clean high- and low-level signal to the output drivers.

Applications Information

Typical shielded twisted pair (STP) and unshielded twisted pair (UTP) cables exhibit skin-effect losses, which attenuate the high-frequency spectrum of a TMDS signal, eventually causing data errors or even closing the signal eye altogether given a long enough cable. The MAX3815 recovers the data and opens the signal eye through compensating equalization.

The basic TMDS interface is composed of four differential serial links: three links carry serial data up to 1.65Gbps each, and the fourth is a one-tenth-rate (0.1x) clock that operates up to 165MHz. TMDS, as with

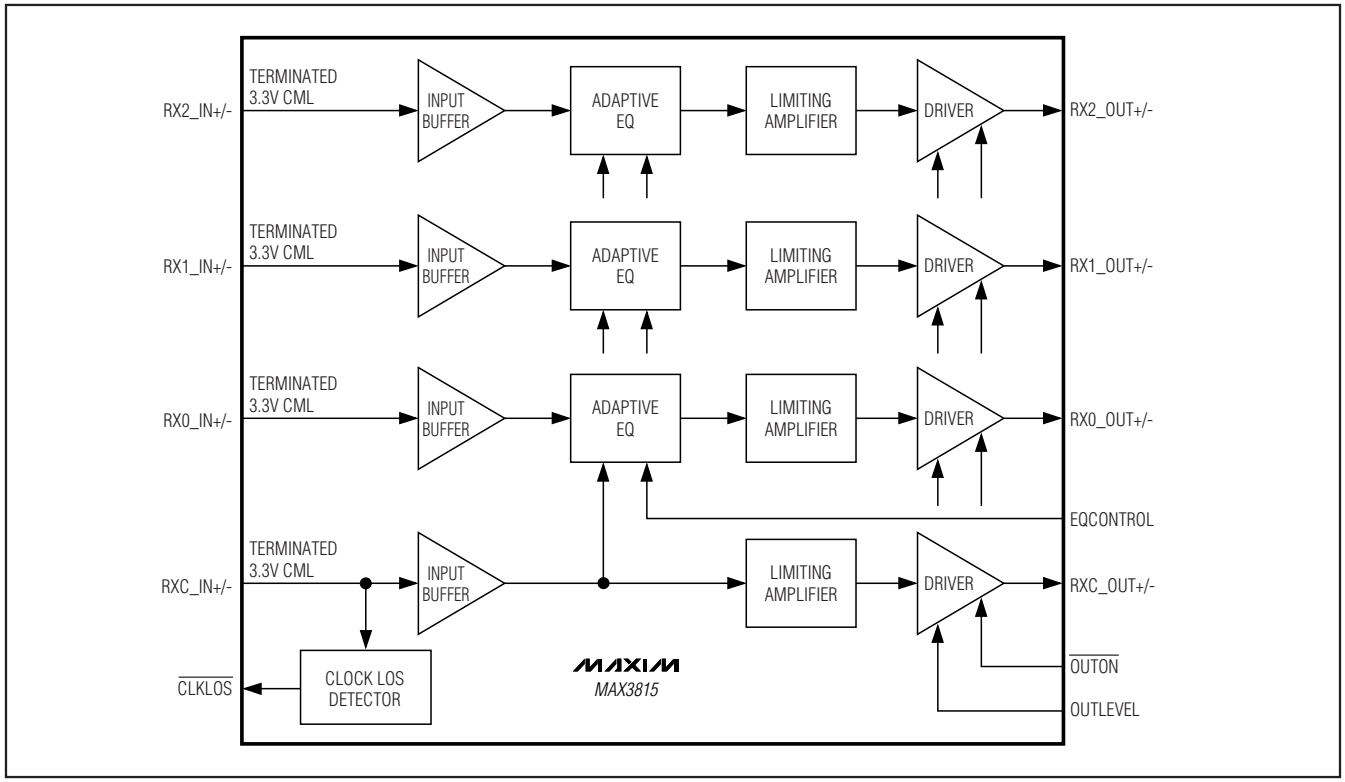


Figure 1. Functional Diagram

analog nVGA links, must handle a variety of resolutions and screen update rates. The actual range of digital serial rates is roughly 250Mbps to 1.65Gbps. For applications requiring ultra-high resolutions (e.g., QXGA), a "double-link" TMDS interface is used and is composed of six data links plus the clock, requiring two MAX3815 ICs with the clock going to both ICs. See Figure 2.

The MAX3815 can be used to extend any TMDS interface as used under the following trademarked names: DVI (digital visual interface), DFP™ (digital flat-panel), PanelLink, ADC™ (Apple display connector), and HDMI (high-definition multimedia interface).

Loss-of-Clock Signal ($\overline{CLKLOS}$) Output

Loss-of-clock signal is indicated by the $\overline{CLKLOS}$ output. A low level on $\overline{CLKLOS}$ indicates that the signal power on the RXC_IN pins has dropped below a threshold. When there is sufficient input voltage to the channel (typically greater than 100mV$_{P-P}$ differential), $\overline{CLKLOS}$ is high. The $\overline{CLKLOS}$ output is suitable for indicating problems with the transmission link caused by, for example, a broken cable, a defective driver, or a lost connection to the equalizer.

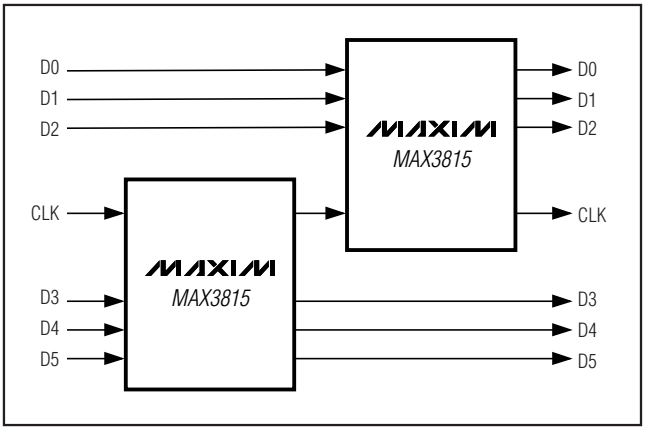


Figure 2. Connection Scheme for MAX3815 in Dual Link Application

ADC is a trademark of Apple Computer, Inc.
DFP is a trademark of Video Electronics Standards Association (VESA).

TMDS Digital Video Equalizer for DVI/HDMI Cables

A squelching function can be created by sending the $\overline{CLKLOS}$ output through an inverter to the $\overline{OUTON}$ pin. This will squelch the CML outputs whenever the clock signal is removed. A loss-of-signal LED indicator can be incorporated into the circuit as well (see Figure 3).

Output Level Control (OUTLEVEL) Input

The OUTLEVEL pin is an LVTTL input that allows the user to select between standard output amplitude (1000mV$_{P-P}$ differential) or one-half output amplitude (500mV$_{P-P}$ differential). Forcing this pin high results in the standard output signal level, and forcing this pin low results in the reduced output signal level.

Equalizer Control (EQCONTROL) Input

The EQCONTROL pin allows the user to control the equalization in one of three ways: forcing the pin to ground sets the equalizer in automatic equalization mode, forcing the pin to V_{CC} / 2 sets the equalizer to minimum equalization, and forcing a voltage between V_{CC} - 1V to V_{CC} allows manual control of the equalization level applied to the input signals. See the *Typical Operating Characteristics* for more information.

Power-Down ($\overline{PWRDWN}$) Input

The $\overline{PWRDWN}$ pin allows the part to be powered down to reduce system power consumption. Force the pin high for normal operation. Force the pin low to power-down the IC. When powered down, the part consumes approximately 10mA.

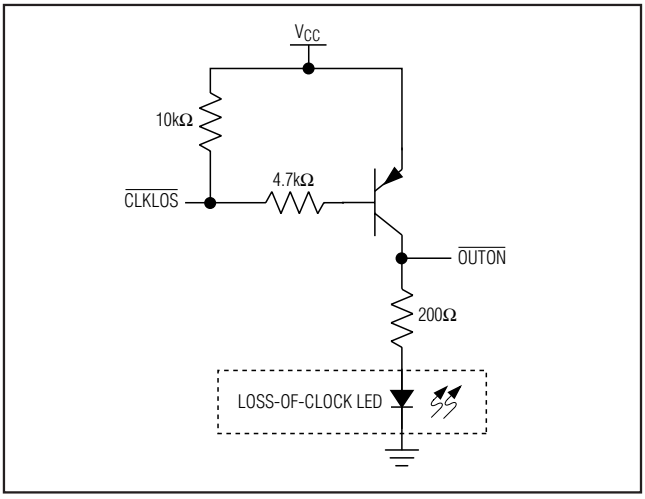


Figure 3. Squelch Circuit

Output On ($\overline{OUTON}$) Input

The $\overline{OUTON}$ pin is an LVTTL input. Force the pin low to enable the outputs. Force the pin high to set a differential zero on the outputs. When disabled, the outputs will go to a differential zero, irrespective of the signal at the inputs.

Cable Selection

TMDS performance is heavily dependent on cable quality. Deterministic jitter (DJ) can be caused by differential-to-common-mode conversion (or vice-versa)

Interface Models

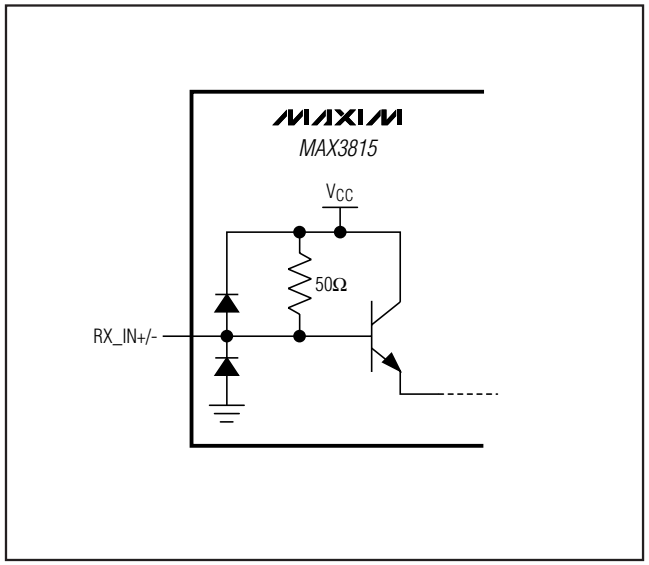


Figure 4. Simplified Input Circuit Schematic

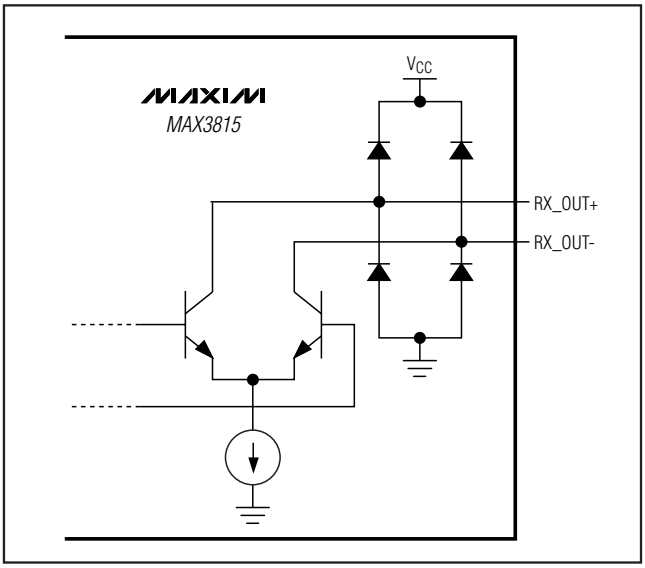


Figure 5. Simplified Output Circuit Schematic

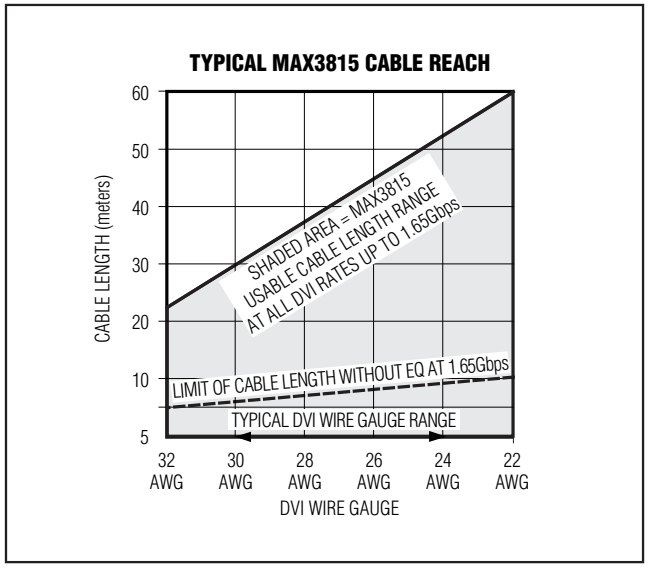


Figure 6. Cable Reach

within a twisted pair (STP or UTP), usually a result of cable twist or dielectric imbalance. Refer to Application Note *HFAN-04.5.4: 'Jitter Happens' when a Twisted Pair is Unbalanced* for more information.

Layout Considerations

The data and clock inputs are the most critical paths for the MAX3815 and great care should be taken to minimize discontinuities on these transmission lines between the connector and the IC. Here are some suggestions for maximizing the performance of the MAX3815:

- The data and clock inputs should be wired directly between the cable connector and IC without stubs.
- Input and output data channel designations are only a guide. Polarity assignments can be swapped and channel paths can be interchanged.
- An uninterrupted ground plane should be positioned beneath the high-speed I/Os.
- Ground-path vias should be placed close to the IC and the input/output interfaces to allow a return current path to the IC and the DVI cable.
- Maintain 100Ω differential transmission line impedance into and out of the MAX3815.
- Use good high-frequency layout techniques and multilayer boards with an uninterrupted ground plane to minimize EMI and crosstalk.

Exposed-Pad Package

The exposed pad on the 48-pin TQFP-EP provides a very low thermal resistance path for heat removal from the IC. The pad is also electrical ground on the MAX3815 and must be soldered to the circuit board ground for proper thermal and electrical performance. Refer to Maxim Application Note *HFAN-08.1: Thermal Considerations of QFN and Other Exposed-Paddle Packages* for additional information.

Chip Information

PROCESS: SiGe BiPOLAR

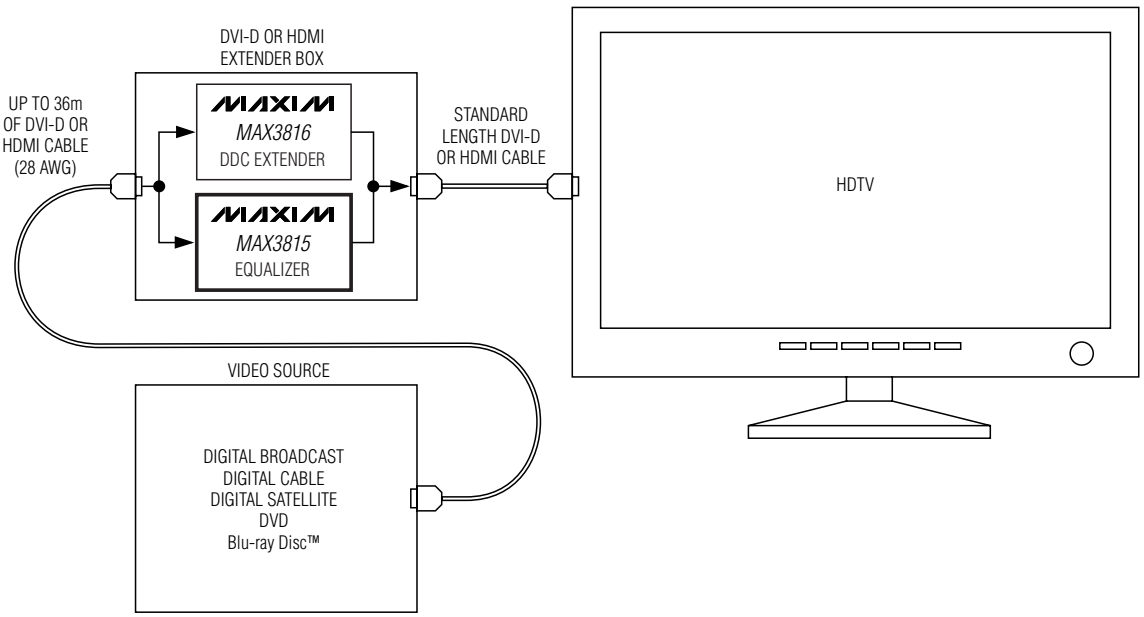
Package Information

(For the latest package outline information, go to **www.maxim-ic.com/packages**.)

PACKAGE TYPE	DOCUMENT NO.
48 TQFP	**21-0065**

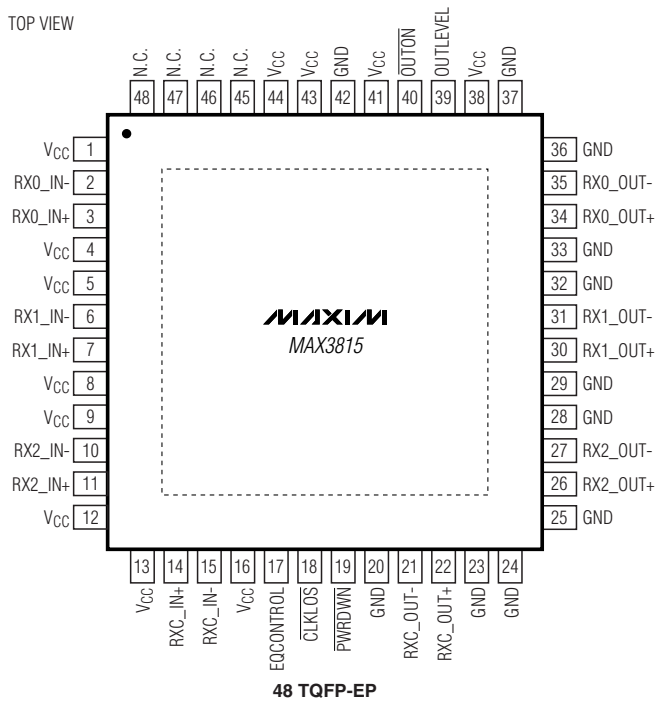
TMDS Digital Video Equalizer for DVI/HDMI Cables

Typical Application Circuits (continued)



Blu-ray Disc IS A TRADEMARK OF Blu-ray DISC ASSOCIATION.

Pin Configuration



48 TQFP-EP

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	10/04	Initial release.	—
1	8/05	Removed future status from the lead-free package in the Ordering Information table.	1
2	2/08	Removed reference to the schematic and board layers in the *Layout Considerations* section.	9

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